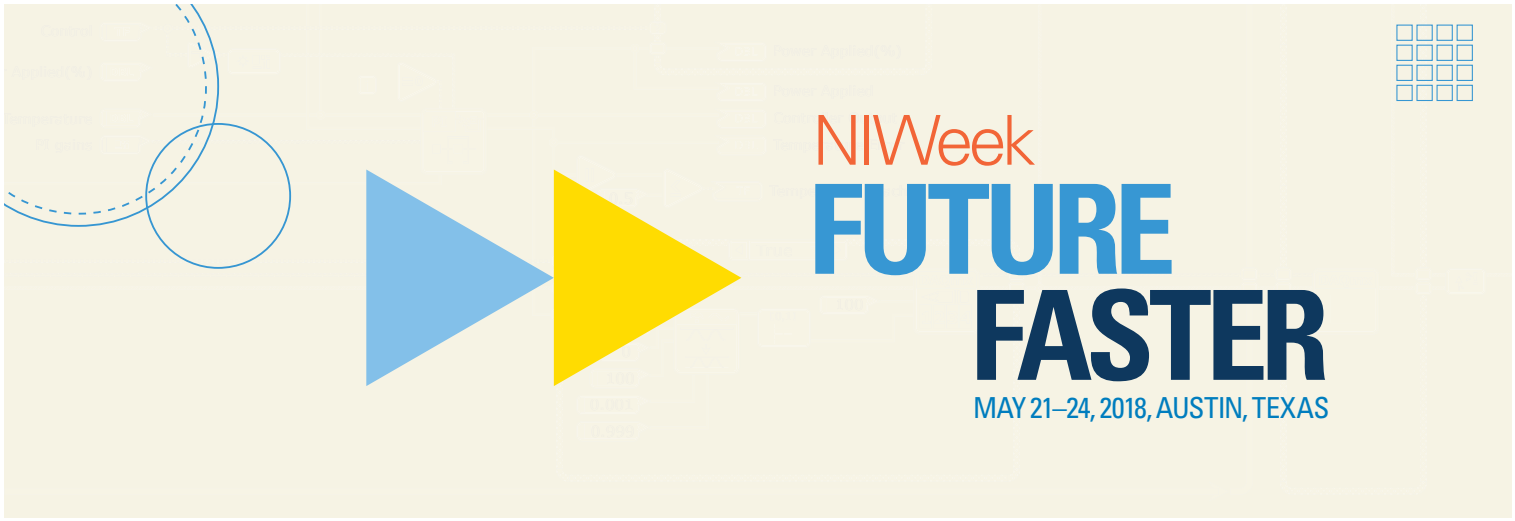

Improving the Semiconductor Design-To-Test Flow

Improving the design-to-test flow requires close collaboration between companies providing electronic design automation tools and automated test solutions. Cadence Design Systems, the leading supplier of analog mixed-signal and RF IC design tools and National Instruments are working together to help improve our customers' design and test experience. Our goal is to improve engineering productivity, improve product quality, and help eliminate design errors. In this session you will hear from both companies about our vision, plans, and the current state of engineering programs in place today.

Session Speakrs

Session Host (National Instruments)

George Zafiropoulos – VP Solutions Marketing, AWR Group

Invited Speakers of Cadence Design Systems

Michael Thompson – RF Solutions Architect

Frank Schirrmeister – Sr. Group Director, System Verification

Yuval Shay – Product Management Director, Analog/Mixed Signal

Design-To-Test Flow Agenda

Tuesday, May 22, Convention Center, Room 2

10:30–10:40 a.m.	Welcome
10:40–11:30 a.m.	Goals & Status
11:30–Noon	Conclusions & Discussion

NATIONAL INSTRUMENTS