AWR®
SIP Flow
White Paper

Malcolm Edwards
AWR Corporation
malcolm@awrcorp.com

UNDERSTANDING AVAILABLE TOOLS FOR RF SYSTEM-IN-PACKAGE AND MULTI-CHIP-MODULE DESIGN AND OPTIMIZATION

RF system-in-package (SiP) and multi-chip-module (MCM) designs present engineers with the challenge of integrating complementary metal oxide semiconductor (CMOS) integrated circuits (ICs) for digital circuits and gallium arsenide (GaAs) or silicon germanium (SiGe) devices for RF and microwave circuits with soft-board laminates and low-temperature co-fired ceramic (LTCC) packages. Software used to design these complex circuits must seamlessly bring together synthesis, simulation, and verification solutions via a single interface in order to ensure optimum component design and placement in each technology. It must also construct schematics and perform physical design entry for any technology in the SiP using uniform commands and menu options.

Unfortunately, this is not usually what the designer experiences, and it is not uncommon for an engineer to design a GaAs chip using one set of IC design tools, Si and SiGe chips with another, and then to integrate both using LTCC or multilayer laminate designed using a printed circuit board (PCB) tool. The architecture of the AWR Design Environment™ (AWRDE) / Microwave Office® software provides the ideal solution to this disjointed approach (Figure 1) by incorporating all of the tools necessary for the design of these complex multi-technology devices within a simple yet comprehensive user interface, enabling faster and more accurate designs from concept through to the system level.

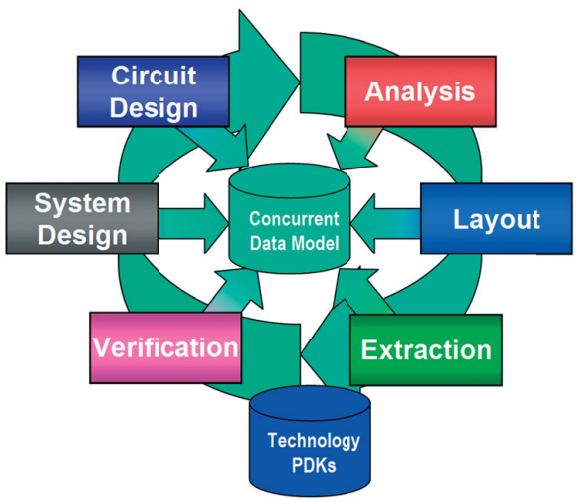

Figure 1. In a concurrent design flow, there are no barriers between technologies and design domains, and all necessary tools are included.

WHAT'S NEEDED

The list of capabilities that a complete and competent environment must possess in order to address the design challenges of RF SiPs and MCMs is comprehensive and includes:

- Steady-state and transient circuit simulation at the component level
- Synthesis tools for filters and matching to aid the analog design process
- High-level system simulation that supports diverse modulation classes
- Component selection from multiple technology libraries
- Support for multiple process design kits (PDKs)
- Graphical display of simulation results and post-processing
- 2D and 3D electromagnetic (EM) simulators
- Circuit extraction in GaAs, silicon, and SiGe in PCB and multi-layer laminates
- Verification tools (ERC, LVS, and DRC)
- Links to downstream manufacturing tools
- A common database using modern object-oriented programming techniques to ensure that the various views of a design are synchronized

The advanced tools and technologies within the AWRDE flow incorporate all of these necessary capabilities, operating smoothly together within a single user interface. A schematic symbol is just one view of a component; the other views include 2D and 3D layouts and the electrical model view. In an integrated design environment, when a component is deleted all the data associated with every view is deleted as well. This obviates the need to synchronize schematic and layout views, enabling a single design engineer to conduct all design activities within a common design framework. This, in turn, reduces layout-versus-schematic (LVS) verification cycles and allows LVS to be pushed out from the design cycle to final verification.

One of the most critical requirements for a modern design tool is support for multiple PDKs. A PDK contains device models and footprints linked by an element symbol as well as drawing layers that define the various process technology layers. The process statistics, material stack-ups, and dielectric and conductor parameters of a particular foundry/manufacturing process are stored in the files that make up a PDK. EDA frameworks have generally supported only a single process, but the advent of the RF MCM and SiP design flow has spurred support for multiple PDKs that enable such heterogeneous designs. For example, AWR's Microwave Office circuit design software supports PDKs from foundries such as WIN Semiconductor and TriQuint Semiconductor, and compound semiconductor device technologies such as GaAs E/D HEMT and SiGe.

The main carrier, such as a multilayer laminate or LTCC substrate, also needs to be defined, unless a SiP is housed in a simple package. When multilayer laminate or LTCC substrates are used, the substrate is not just the carrier and interconnect matrix, but is also used for buried passives and surface-mount device attachments. As such, this gives the SiP designer considerable freedom in component selection and placement. For example, an inductor needed as a bias choke could be placed on a semiconductor chip, buried in the substrate as a multi-layer spiral, or incorporated as a wound-inductor surface-mount device. Only a design environment that supports all factors up for consideration can provide fast and efficient trade-offs of assembly limitations, inductor Q, self-resonant frequency, reliability, as well as assembly and parts cost.

DESIGN TASKS: BOTTOM UP

As the SIP's operating frequency and its need to handle diverse signals increase, track layout and modeling of the circuit interconnect become critical. AWR's software supports two approaches to the issue of interconnect design. The first is the traditional use of microstrip, coplanar waveguide, and stripline for critical interconnects and the second is a more PCB-like or silicon IC-centric wiring approach using AWR's unique Intelligent Nets™ (iNets) technology.

An iNet can be thought of as an interconnect element displayed as a trace or path in a layout view and a wire within a schematic view. Therefore the iNet can be modeled using either a simple DC connection, an intermediate model such as a combination of RLCK, or a fully-dispersive microstrip model. If none of these approaches are adequate for the given interconnect geometry, the iNet can then be modeled using an EM-based extraction process. This more detailed and higher accuracy approach may be appropriate and/or necessary if unintended coupling between tracks significantly impacts circuit performance or there are defects in the ground plane.

AWR's innovative new ACE™ (automated circuit extraction) technology is part of the suite of extractors available within the AWRDE. ACE leverages proven digital and analog mixed-signal (AMS) circuit extraction techniques from physical layout, but incorporates microwave models and high-frequency principles. Rather than packaging up the geometry of the interconnect and sending this data to a 3D-planar method-of-moments (MOM) solver, or a 3D-arbitrary finite element method (FEM) or finite-difference time-domain (FTDT) solver, the data is used to generate an equivalent circuit based on a set of user-defined rules.

Figure 2 shows a simplified section of a multi-layer circuit board's interconnect, minus the surface-mount components. This example does not detail any buried passive components, but the complexity is nevertheless typical of many advanced SiP and module designs. The buried passives could be modeled using a set of S-parameters in the case of complete functional blocks such as diplexers, or have scalable compiled models in the case of discrete components such as polymer thin-film capacitors or buried spiral inductors. A typical SiP design that includes Si, GaAs, and SiGe in a multilayer laminate is shown in Figure 3.

There are some hidden benefits to using the iNet approach alongside ACE. Not only is the physical design entry more straightforward, but when coupled with an automated extractor, the designer can tackle optimization and yield analysis rapidly - without a considerable amount of time for detailed EM analysis. As such, yield is not relegated to a downstream verification process with its attendant inefficiencies, but rather becomes an up-front design task.

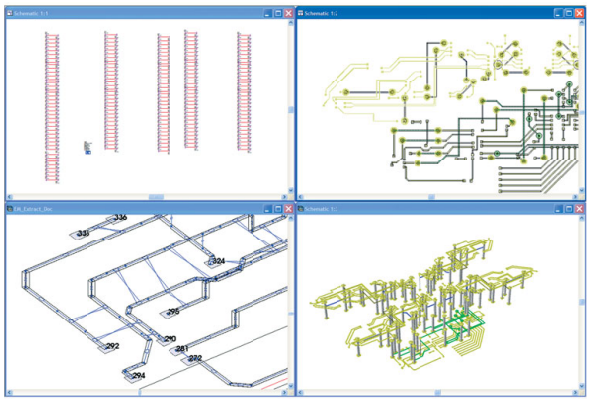

Figure 2. A 16-layer circuit board with 168 iNet interconnects that were extracted using ACE.

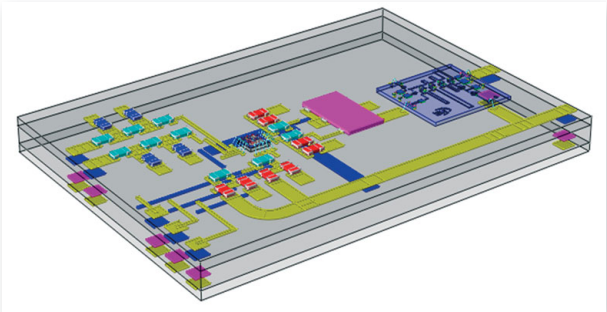

Figure 3. A SiP design that encompasses three technologies: Si, GaAs, and multilayer laminate, each one using iNETs to define the circuit interconnects.

Digital and AMS extractors typically use RLCK models to model interconnect-reduced geometries. However, they require very dense networks at microwave frequencies to capture dispersion and skin-effect and tend to be bandwidth-limited. In contrast, ACE algorithms view the layout in terms of distributed lines, coupled-lines, and discontinuity models that microwave engineers have used and trusted for years (such as MLIN/SLIN, MTEE/STEE, and M2CLIN/S2CLIN), rendering dispersion, skin-effect, and bandwidth as non-issues.

Moreover, vias can be modeled with S-parameter files from pre-defined libraries, a fixed resistance, or an AWR via model. EM analysis can also be used when some shapes cannot be reduced to these accepted microwave elements. The goal is to use more complex and accurate tools only when required, maintaining fast and efficient design entry and analysis processes for as long as possible. The ACE tool automatically generates a detailed, extensive netlist in seconds for complex arrangements of interconnects that engineers typically would formerly spend many hours or days manually creating.

When EM analysis is used to provide a definitive view of circuit performance, it must support internal self-calibrated EM ports. These ports allow the traces used as interconnects between the surface-mount devices and semiconductor chips to be extracted for EM analysis in an automated fashion. The data sent back from the solver is then automatically stitched into the circuit solver with minimum involvement on the part of the designer.

Figures 4a and b illustrate the two classes of EM-related simulation performed on a simple single-die SiP: ACE and AXIEM™ (AWR's 3D planar EM tool) respectively. The ACE view (4a) shows the extracted models from the geometry. With the AXIEM view (4b), the mesh has not been decimated to reduce the number of unknowns. The individual traces have been color-coded to assist in a first-pass layout vs. schematic (LVS) verification. The figures demonstrate that without the need to invoke a short or open checker, or conduct a full LVS, wiring errors can quickly be spotted and repaired.

In many SiP designs, a single module must accommodate RF and microwave and high-speed digital signals. For the high-frequency tracks, the circuit interconnect will most likely have been designed using high-frequency elements (MLINS, etc.), but for high-speed digital signals, iNets are more likely to have been used. Another difference between the analog and digital design methods are the classes of models employed.

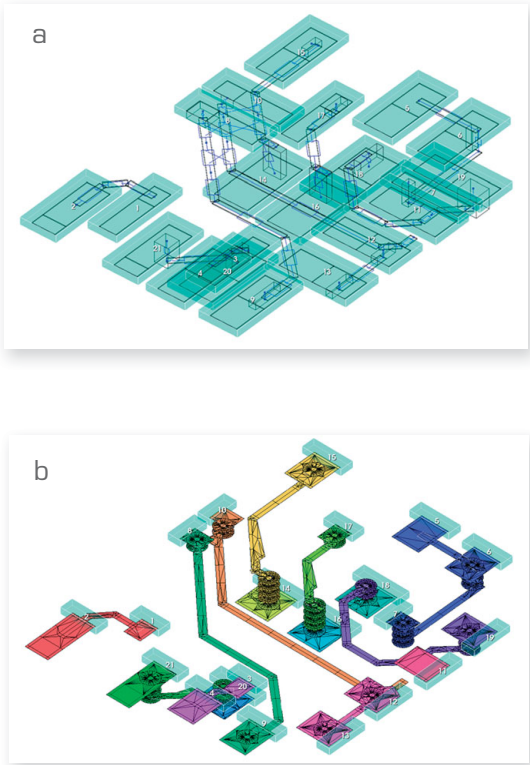

Figure 4. ACE (a) and AXIEM (b) simulations of a single-die SiP with its surface-mount devices hidden.

For the analog high-frequency components, behavioral models, S-parameters, or detailed circuit descriptions are used, and for the digital content the input/output buffer information specification (IBIS) model is better suited as it defines the terminal behavior of such components. With IBIS models, designers can explore the waveform degradation caused by track parasitics and the parasitics associated with the packaged components (Figure 5).

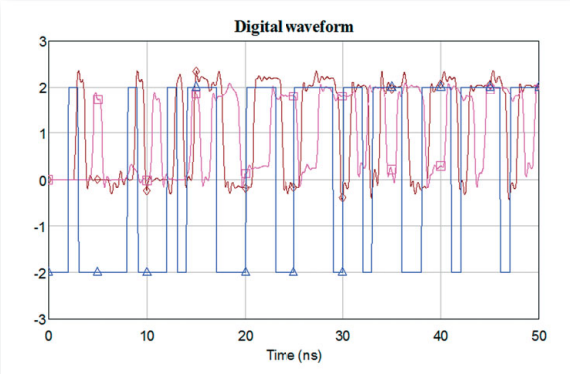

Figure 5. Transient simulation using an IBIS model for the chip's IO pins.

DESIGN TASKS: TOP DOWN

Before the aforementioned chip and package work can be undertaken, the system architecture must be defined, which involves partitioning the processing blocks (amplifiers, filters, mixers, AGC…) between one or more technologies. More than one technology may be considered as a suitable solution for some blocks. Risk reduction, time to market, and the demands made by customers all play a role in shaping the SiP's architecture. AWR's Visual System Simulator™ (VSS) tool was created for just such system architecture evaluation, and it can be an invaluable tool for ensuring that a communications, radar, or other type of system is optimized to achieve its best performance. VSS's two major technologies are RF Budget Analysis™ (RFA) and RF Inspector™ (RFI) and are of great benefit to the design of multi-band, multi-waveform systems. RF Budget Analysis includes features such as statistics and yield, accounting for image noise in mixers, and the ability to tune parameters in order to get an instant feel for system performance.

By adding the effects of voltage standing wave ratio (VSWR) interaction between the analog stages of the system, the designer can gain insight into the spread in gain, noise figure, two-tone, and third-order intercept point, and define the gain adjustments (if necessary) for the design at the point of manufacture. VSS is seamlessly integrated into AWR's Microwave Office design environment, so that simple behavioral models can be swapped out for circuit-based models and/or replaced with measured data. A VSS screen shot showing RF Budget Analysis with statistical variation and its effect on system gain is shown in Figure 6.

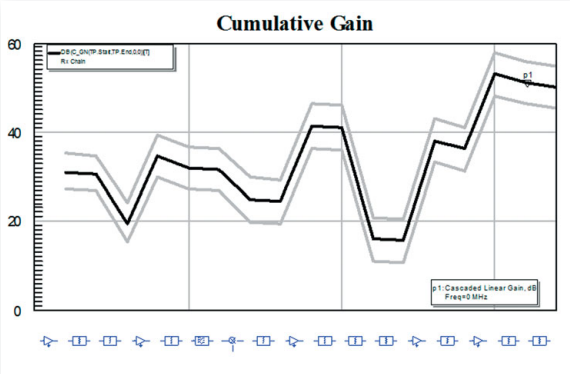

Figure 6. RF Budget Analysis with statistical variation and its effect on system gain.

In parallel with RF Budget Analysis, potential signal integrity issues should be investigated. Increasing the number of frequency conversions may increase the degrees of freedom in synthesizer design, but with penalties in cost, complexity, and spur-generation. Using the same system diagram, it is possible for the system engineer to examine the spur growth and identify areas for improved screening or filtering.

In the context of a SiP, the screening can be resolved by assigning certain conductor layers for ground plane floods. Other conductor layers can then be reserved for critical signal-carrying tracks.

The feature within the VSS software that performs this analysis is RF Inspector. Figure 7a is a VSS screen shot showing wanted and unwanted signals in a double-conversion receiver. Figure 7b shows the data gathered after selecting a specific spur. It includes a partial heritage of the wanted signal and the data associated with unwanted tones. Understanding the heritage of each signal is critical in order to design a robust system and is aided by the VSS sophisticated reporting process. Having defined a system architecture that satisfies the basic requirements for system gain, noise figure, and third-order intercept point, it is necessary to investigate the transport of customer data. This can be accomplished within the VSS test bench function such as one for Mobile WiMAX shown in Figure 8.

CONCLUSION

The design of RF MCMs and SiPs is a broad and diverse process that ranges from detailed circuit design to complex system design. Because these complex circuits encompass multiple semiconductor technologies and perform a variety of functions over a broad array of frequencies, it is essential that the EDA environment used to design them be based on a single architecture and a uniform approach to design entry and simulation. It must also include circuit, system, and EM simulators, all integrated within a straightforward but comprehensive user interface. The AWRDE embodies all of these attributes, and, when combined with the system-level analysis abilities of VSS software, makes it possible to efficiently design, analyze, and optimize the performance of RF MCMs and SiPs for wireless communications applications.

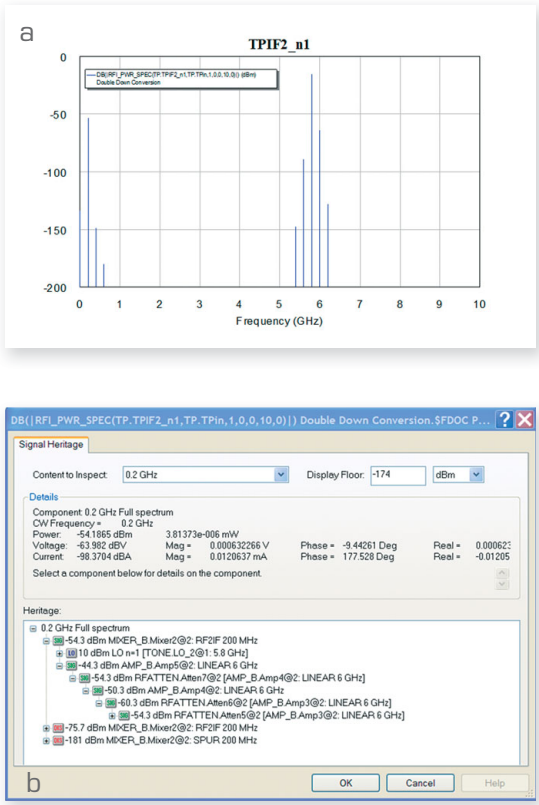

Figure 7. RF Inspector depicts wanted and unwanted signals in a double-conversion receiver (a) and in greater detail after selecting a specific spur (b). The latter includes a partial heritage of the desired signal and the data associated with unwanted tones.

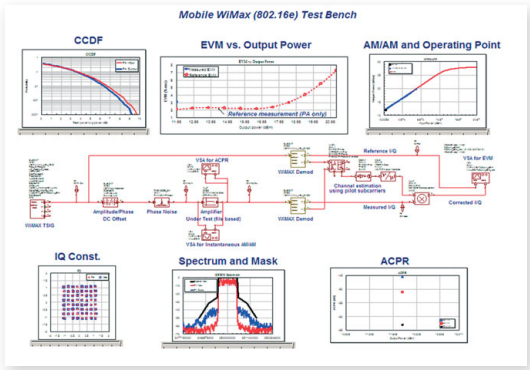

Figure 8. The Mobile WiMAX test bench within VSS.

AWR, 1960 East Grand Avenue, Suite 430, El Segundo, CA 90245, USA
Tel: +1 (310) 726-3000 Fax: +1 (310) 726-3005 www.awrcorp.com