

# Datasheet

## PDKs for ON Semiconductor



NI AWR Design Environment supports several ON Semiconductor process design kits (PDKs) for use by mutual customers. These PDKs offer:

- Symbols and schematics (Cadence compatible)
- Fully-scalable layout PCells
- Advanced layout utilities
  - Automatic slot insertion
  - Connectivity checking/highlighting
- Accurate EM simulation featuring:
  - Pre-defined substrate definitions and stackups
  - Pre-configured simulation settings
- Design examples and tutorials

Current PDKs include:

Process	Description
IPD1	Two layer process, optional 9 $\Omega$ /sq resistor, capacitor (0.62 nf/mm <sup>2</sup> ), High-Q™ inductor and aluminum bond pad finish
IPD2	Three layer process, optional 9 $\Omega$ /sq resistor, capacitor (0.62 nf/mm <sup>2</sup> ), High-Q inductor and aluminum bond pad finish

ON Semiconductor IPD PDKs work seamlessly with the latest version of NI AWR Design Environment. Contact your local [NI AWR software representative](#) for more information or visit ON Semiconductor at [onsemi.com/PowerSolutions/content.do?id=16699](http://onsemi.com/PowerSolutions/content.do?id=16699) for additional details.

[ni.com/awr](http://ni.com/awr)

