Steady State and Transient Thermal Analyses of GaAs pHEMT Devices

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Abstract— GaAs pHEMT thermal reliability test structures are introduced which incorporate on-wafer heating using Thin Film Resistors (TFR) and a DC gate metal temperature measurement method. Results from 3D Finite Element Method (FEM) thermal simulations are compared with measurements and used to investigate the frequency response of device self-heating. Comparisons are made with existing thermal models. The influence of individual device structures on the thermal characteristics of an entire device is investigated and the epitaxial layers are seen to have a large impact on overall performance. Bias dependent self-heating, independent of thermal dissipation is observed and attributed to confinement of the thermal source as the drain voltage is increased.

Keywords-Thermal test structure; wafer level; thermal modeling; temperature measurement; pHEMT channel temperature.

I. INTRODUCTION

Thermal effects in electronic devices are studied to investigate their influence on reliability and electrical performance. Due to the decreasing size of semiconductor devices operating at unchanged power levels, thermal analyses provide circuit designers with important information about device degradation and electro-thermal coupling. Steady state thermal analyses have been performed for many years in electronics reliability engineering to evaluate device lifetimes. Device channel temperature is the most critical parameter to determine in such a reliability study as it is the primary source for thermal degradation mechanisms. Many techniques exist for modeling and measuring device channel temperatures, however large discrepancies are reported in the literature [1].

While steady state simulations are useful in the case of device lifetime studies, they provide no information about the dynamic behavior of devices which is important in high power density applications employing complex signals. Transient thermal analyses can be used to model the self-heating occurring in devices under these conditions and help determine the implications for circuit performance. An example of this electro-thermal coupling has been shown in the relationship between self-heating and Intermodulation Distortion (IMD) [2]. A comprehensive study on this relationship showed that by investigating a device's IMD across a range of bias conditions and tone spacing, the thermal transfer function of the device can be extracted [3]. The thermal analysis in the study was performed as a rudimentary finite difference problem of a heat source (resembling a gate finger) centered on a GaAs substrate. It did not include details about the device metallization, heat flow to air, or precise details about device geometry.

This paper presents a detailed study of steady state and transient thermal analyses on a range of GaAs pHEMT devices. Thermal simulations are performed with Capesym's SYMMIC^{TM}. It is a template based 3D FEM thermal simulator for monolithic microwave integrated circuits which allows the user to precisely define a semiconductor device's material composition and geometry. Measurements accompany steady state simulations, while a simulated transient response is fit with an empirically determined function from a previous study as well as an IMD simulation using experimentally extracted data [4].

Section II discusses steady state simulations performed with SYMMIC^{TM} to determine the average gate metal temperature of pHEMT devices. The results are compared to direct measurements of device gate metal temperatures. With agreement between simulations and measurements one can use the thermal model to infer peak temperatures in the device's channel region under typical bias conditions.

In section III, an electro-thermal simulation is reported. Results from transient thermal simulations of GaAs pHEMTs are discussed and compared to an existing heating model used in the precise simulation of intermodulation products [4]. Simulations are then presented which investigated the effects of individual structures (e.g. vias, passivation, epi layers) on a device's thermal frequency response.

II. STEADY STATE THERMAL ANALYSES AND MODEL CALIBRATION USING EXPERIMENTAL RESULTS

A. Simulations to Determine Average Gate Metal Temperature

Simulations were performed to contribute to a reliability study on a WIN Semiconductor Co. Ltd. 0.15 μm GaAs pHEMT process. In accelerated lifetime tests, devices are commonly stressed thermally and the associated degradation in GaAs FETs is dominated by gate sinking [5]. The temperature at the Schottky barrier, where the gate metal meets the epi layers, determines the rate of gate sinking [1]. As a calibration procedure, agreement was sought for average gate metal temperature between simulations and measurements before calculating the peak channel temperature from the simulations. A 2×100 μm pHEMT simulation template was configured to include full

metallization, passivation, epi layers, 100 μm thick substrate, vias, and base plate adhesive. The template is illustrated in Fig. 1. It was used to simulate what will be described here as a conventional thermal test structure. A 50 nm × 500 nm × 30 nm mesh was defined in the channel heat source region and a constant base plate temperature was defined.

For 135 mW DC dissipation and a 22 °C base plate temperature, simulations returned an average gate metal temperature of 67.82 °C. With the same power dissipation and a base plate temperature of 70 °C, the simulated average gate metal temperature was 118.92 °C. The resulting gate metal temperature profile is shown in Fig. 2. The temperature peaks at the center of the gate finger and is seen to be lowest at the end attached to the gate bus metal, owing to the increased thermal sinking.

A novel device configured for wafer level reliability studies was also simulated and later fabricated for measurements using the same fabrication process as the conventional thermal test structures. The design was modified from a previous reliability study [6] to permit channel temperature measurements by wafer probing. Its geometry differed to the conventional thermal test structure by the inclusion of a TFR between the source and via as illustrated in Fig. 3. The role of the TFR is to provide excess heating required for the accelerated onset of gate sinking. It was positioned to be as close as possible to the gate metal. Air bridges were used to make the connection between sources and vias.

The simulation of the TFR heated structure with no power dissipated in the TFR returned an average gate metal temperature of 68.07 °C with 135 mW dissipated in the FET channel and 22 °C base plate temperature. With the same power dissipation and a base plate temperature of 70 °C, the average gate metal temperature was 119.56 °C.

B. Temperature Dependent Gate Resistance Measurements

Measurements were performed on both conventional and TFR heated thermal test structures. They consisted of 2x100 μm GaAs pHEMTs, each having modifications to
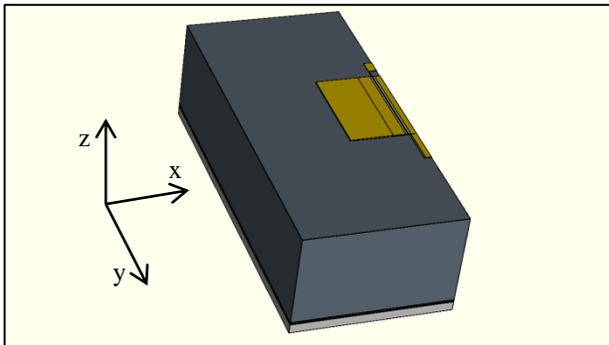

Figure 1.   The SYMMIC^{TM} 2x100 μm pHEMT template used to simulate gate metal temperatures of conventional thermal test structures.
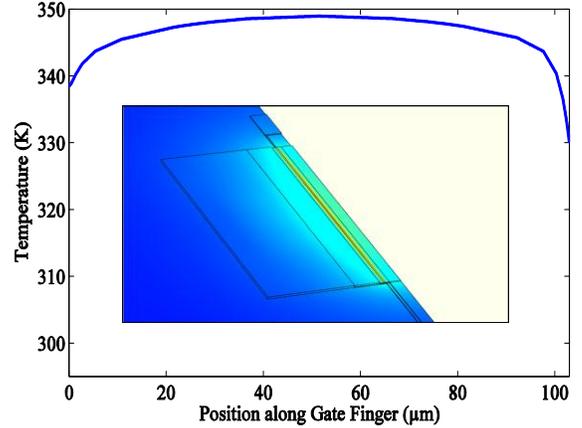

Figure 2.   Simulated gate metal temperature profile for 135 mW power dissipation in the pHEMT channel and a base plate temperature of 22 °C. The inset figure shows a simulated template.
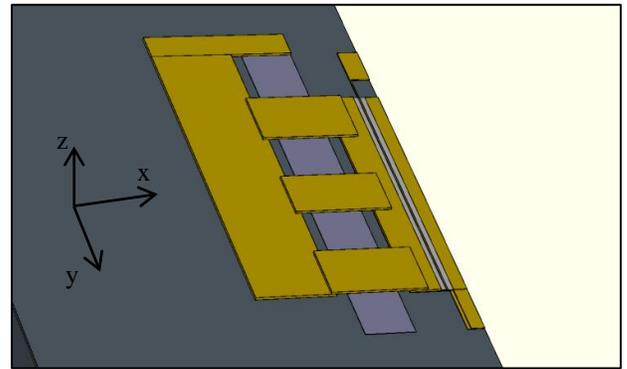

Figure 3.   Template used for simulating the average gate metal temperature of the thermal test structure incorporating TFR heating.

enable 4 terminal Kelvin measurements of average gate metal temperature [1],[7]. Fig. 4 illustrates the fabricated wafer level reliability structure combining TFR heating with gate resistance measurement capability.

The thermal response of the devices' gate metal resistance was calibrated using a thermal chuck and measured to be linear between room temperature and 100 °C [1]. Gate metal temperatures were measured as functions of power dissipation in the FET devices and also of power dissipation in the TFR when present.

Power dissipation in the pHEMT was increased by raising the drain voltage over constant gate voltage. Fig. 5 shows close agreement between simulations and measurements at low power dissipation. However, at higher power levels the simulations return lower temperatures than the measurements. This level of discrepancy was found across all of the devices tested. The thermal model used in this study has fixed heat source dimensions regardless of bias. However, at higher drain voltages the electric field becomes more localized at the gate edge on the drain side leading to elevated temperatures [7].
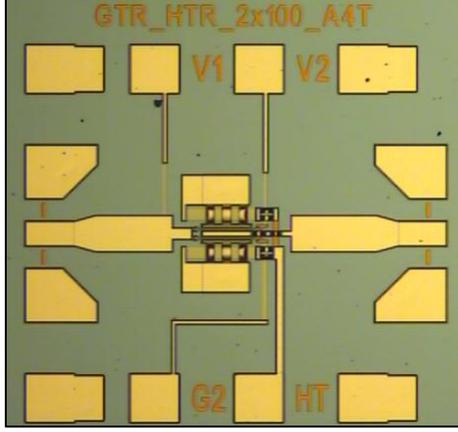
Figure 4. The fabricated thermal test structure with TFR heating capability for on-wafer accelerated lifetime testing.

To improve the accuracy of the simulations a bias dependent correction factor may be applied [8].

The measured average gate metal temperature of the conventional thermal test structure biased for 135 mW dissipation with a 22 °C base plate temperature was 74.77 °C. For a 70 °C base plate temperature the measured average gate metal temperature was 129.98 °C.

Measurements were made on the TFR heated thermal test structure for three separate cases to study heat sources individually as well as when coupled. Fig. 6 shows close agreement between measurements and simulations for the case where the TFR is biased while the FET is unbiased. This further supports not only the thermal model and simulations but also the bias dependence of FET self-heating seen in previous measurements. These results as a whole are summarized in Table I. Also included are the simulated maximum Schottky junction temperatures which may be used in statistical analyses to determine device lifetimes. The TFR heated structure's average gate metal temperature was measured to be 252.98 °C with the base plate temperature at 70 °C, 135 mW dissipated in the FET channel and 1.554 W dissipated in the TFR heaters which corresponds to the maximum current density for reliable operation. While this gate metal temperature is adequate for lifetime testing [5],[6], higher temperatures can be accessed by increasing the base plate temperature. Foundry reliability studies on the TFR found that there were no significant changes to the sheet and contact resistances after 1000 hrs at 280 °C.

The FET templates used in the simulations approximate the epi layer composition using 3 layers (GaAs, GaAs and AlGaAs). A real pHEMT may have a superlattice structure consisting of thin alternating layers of semiconducting material. This would result in a thermal conductivity much lower than the bulk values which implies that epi layers have a significant impact on the thermal performance of devices [9]. Information regarding the physical properties of the epi layers in devices is not made readily available by most foundries. Therefore to achieve agreement between simulations and measurements the thickness of the epi layers in the templates were calibrated accordingly.

As a further test for the thermal model, 2×100 μm FETs with gate resistance measurement contacts were designed and fabricated using a different, but similar, WIN Semiconductor 0.15 μm GaAs pHEMT process. Its substrate was 50 μm thick and the vias used were half the size of the previous process. Examples of these devices are shown in Fig. 7. The value of gate to gate spacing was set at 17.5, 20 and 25 μm to investigate the thermal coupling of device heat sources. Measurements returned marginally hotter temperatures for closer spaced gate fingers. Upon setting the device template geometries and tuning the epi layer thicknesses, the simulations accurately modeled the temperature measurements. The temperature changes seen due to the variation of gate finger spacing were resolved providing confidence in the heat spread modeling and calibration procedure. The results are presented in Table II.

Finally, for each value of gate finger spacing, Fig. 8 illustrates the dependence of the thermal resistance R_{th} on power dissipation P at a fixed gate voltage. Thermal resistance is calculated as

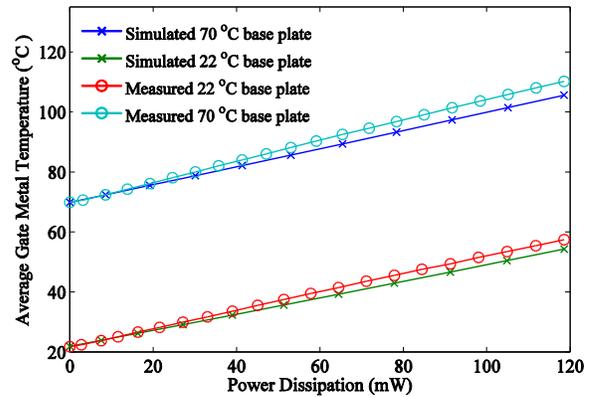$$R_{th} = \frac{T_{gate} - T_{bp}}{P} \qquad (1)$$

Figure 5. Measured average gate metal temperature varying with power dissipation for a conventional thermal test structure. Drain voltage was stepped in increments of 0.25 V. Gate voltage was held constant.
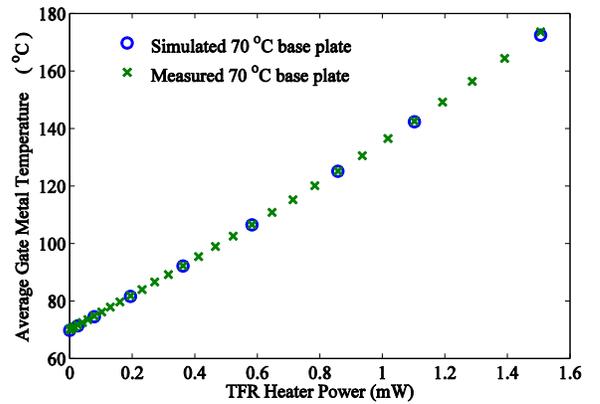

Figure 6. Average gate metal temperature as a function of total power dissipated in the TFR heaters. No power is dissipated in the FET channel.

TABLE I.   **Comparison of Simulations and Measurements of Conventional and TFR Heated Thermal Test Structures.**

Thermal Test Structure Type	Base plate Temperature (°C)	Power Dissipated in FET channel (mW)	Power Dissipated in TFR (mW)	Simulated Average Gate Metal Temperature (°C)	Measured Average Gate Metal Temperature (°C)	Difference (%)	Simulated Maximum Schottky Barrier Temperature (°C)
Conventional	22	135	N/A	67.82	74.77	- 9.3	77.48
Conventional	70	135	N/A	118.92	129.98	- 8.5	129.10
TFR Heated	22	135	0	68.07	67.19	+ 1.3	78.27
TFR Heated	70	135	0	119.56	120.89	- 1.1	130.38
TFR Heated	70	0	1506	172.42	173.69	- 0.7	180.36
TFR Heated	70	135	1554	233.45	252.98	- 7.7	253.90

TABLE II.   **Comparison of Simulations and Measurements of Conventional Thermal Test Structures with Varied Gate Finger Spacing.**

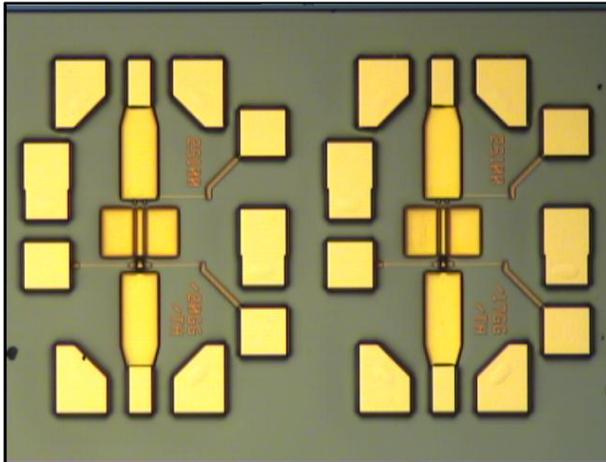| Finger Spacing (μm)	Base plate Temperature (°C)	Power Dissipated in FET channel (mW)	Simulated Average Gate Metal Temperature (°C)	Measured Average Gate Metal Temperature (°C)	Difference (%)	Simulated Maximum Schottky Barrier Temperature (°C)
17.5	22	100	53.22	57.67	- 7.7	60.10
17.5	70	100	103.51	109.78	- 5.7	110.79
20	22	100	52.82	55.67	- 5.1	59.66
20	70	100	103.06	107.54	- 4.2	110.29
25	22	100	52.18	54.84	- 4.9	58.91
25	70	100	102.34	106.44	- 3.9	109.45

Figure 7. Thermal test structures from a different fabrication process with varying gate finger spacing. Substrate thickness and via dimensions are half the size of those in Fig. 4.

Figure 8. Thermal resistances varying with gate finger spacing.

where T_{gate} is the average gate metal temperature and T_{bp} is the base plate temperature. While not carried out here, a similar test on devices with many gate fingers would be expected to produce a larger temperature shift due to the multiple heat sources in a confined thermal space. The negative slope seen in the thermal resistance at higher drain voltages suggests that space charge limited current is involved. As the carrier velocity saturates at the drain end of the device the electron density becomes higher increasing the output conductance of the device. As the gate voltage is increased this slope becomes more positive and the values of thermal resistance decrease.
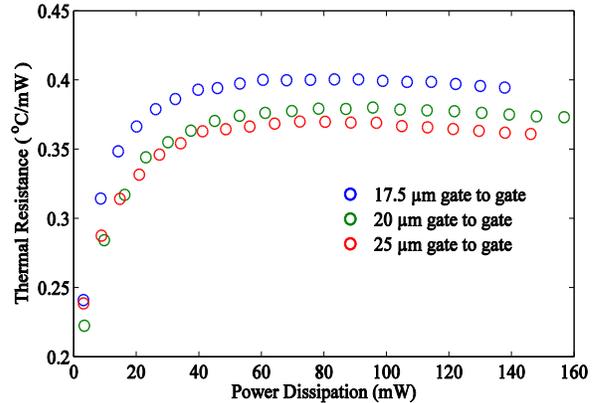
III. TRANSIENT THERMAL ANALYSES TO DETERMINE DEVICE THERMAL FREQUENCY RESPONSES

Intermodulation measurements were previously performed on FET devices by Parker and Rathmell [4],[5]. The devices were biased in a region which produced a deep null in the intermodulation level. With the device at this operating point, the electrical contribution to the IMD measurement was highly suppressed leaving the mechanism of self-heating to dominate. As the tone spacing was varied, the IMD level responded according to the device's thermal resistances and capacitances. The thermal frequency response was modeled with a low pass function $H(\omega)$ as it fit well with simulations:

$$H(\omega) = \frac{1}{\left(1 + {j\omega}/{\omega_a}\right)^n \left(1 + {j\omega}/{\omega_b}\right)^{(1-n)}} \qquad (2)$$

where ω_a and ω_b are the lower and upper roll off frequencies respectively and n is the order of the response which is seen to be sub first order. The function was originally used to fit a finite difference model of a FET consisting of a planar heat source on a uniform substrate with no details of metallization, passivation or epi layers. In this work SYMMIC^{TM} was used to verify the electro-thermal model and to investigate the effects of individual device structures on thermal frequency responses.

A. FEM Verification of an Existing Heating Model and Comparison with an Experimentally Extracted Non Linear Electro-Thermal Device Model

A SYMMIC^{TM} template was configured to perform a transient thermal FEM simulation of a 2×100 µm GaAs pHEMT device including metallization, passivation and epi layers. It consisted of a 100 µm thick GaAs substrate with a boundary extending 1000 µm on each side. An instantaneous power step of 50 mW was dissipated in the channel. Using a logarithmically spaced time data set, the transient response of the device was simulated to investigate its thermal behaviour between 100 Hz and 100 GHz. The resulting step response of the channel heating was differentiated to obtain the impulse response. A suitable FFT was applied to the impulse response to obtain the frequency response [10].

To predict IMD, an electro-thermal model incorporating not only thermal IMD capability [4],[5], but also other IMD contributors, such as impact ionization [11] and trapping [12] was used within a multi-tone harmonic balance simulation. The model, extracted from measured data [13] for this particular device has a low end roll off frequency of approximately 10 kHz and the order is 0.14. In order to emphasize the thermal transient effects, the drain voltage was set at a value to minimize impact ionization, and for several decades of tone spacing the gate voltage was swept in a region near pinch off. In this region the effects of trapping were minimized and the envelope of the IMD response follows the thermal response. The results are illustrated in Fig. 9. The deviations seen in the SYMMIC^{TM} response are mostly due to the inclusion of epi layers but also passivation and metallization. SYMMIC^{TM} also returns a more gradual high frequency roll off than $H(\omega)$.

B. Effects of Device Structures on Thermal Frequency Response

The inclusion of metallization, passivation and epi layers in the device template introduces complexities that produce less uniform heating than the simplified case of a heat source on a substrate. The thermal transfer function of a 2×100 µm pHEMT was investigated upon removal of individual device structures. Fig. 10 illustrates the step response of each simulated case. Fig. 11 shows the corresponding frequency responses. Results are normalized with respect to the full template simulation.

Table III summarizes the results from the study. The most significant effects were seen upon removal of the passivation layer, the gate T metal and the epi layers. While removal of many of these structures is not possible in
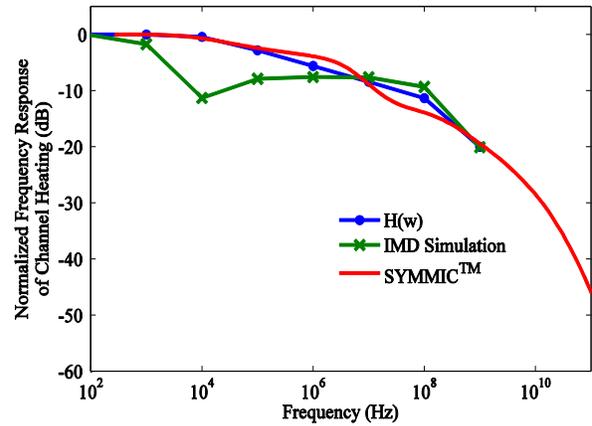

Figure 9. Frequency response of heating for a 2x100 µm GaAs pHEMT. The SYMMIC^{TM} response is compared to a full electro-thermal model and $H(\omega)$.

practice (to retain a working FET), the simulations highlight the importance of their inclusion in the model. The removal of the epi layers, in particular, drastically decreases the simulated channel temperature across almost the entire spectrum. This is due to the lower thermal conductivity of the epi layers compared to that of the GaAs substrate.

The removal of the entire drain and source metal was seen to have a much more significant impact on channel temperature rise than the removal of the cap layer alone. A peak channel temperature rise of 18% between 100 Hz and 400 kHz was seen in their absence. This has far reaching implications for FET gate pitch in power amplifiers.

C. Trade-off Studies

SYMMIC^{TM} was used to perform a study comparing the thermal effects of vias and passivation on a device with and without a BCB layer. Fig. 12 shows results from simulations involving a 2×100 µm GaAs pHEMT. Results are normalized with respect to the full template simulation. The addition of BCB does not have a significant effect on the frequency response from 200 Hz to 20 kHz. This was
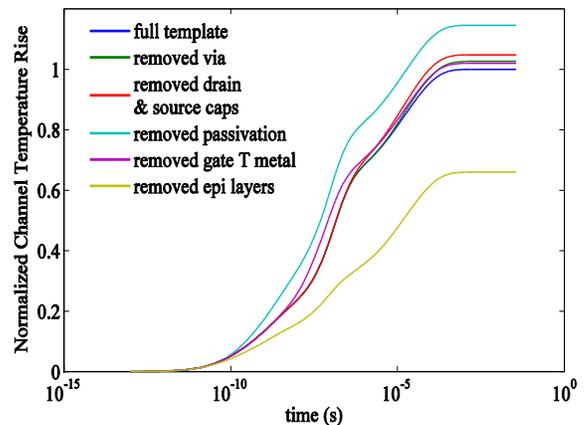

Figure 10. Step responses of the various template configurations to investigate the thermal effects of individual device structures.
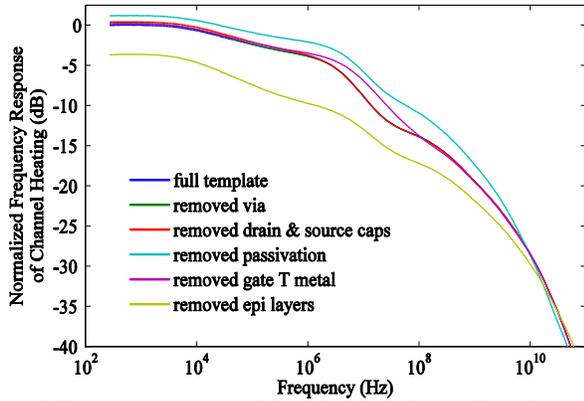
Figure 11. Frequency responses of the various template configurations to investigate the thermal effects of individual device structures.

Figure 12. Trade off study for the inclusion of passivation, vias and BCB in the FET model.

TABLE III. Summary of the Effects of Individual Device Structures on the Thermal Frequency Response

Structure Removed	Frequency Range of Most Significant Impact	Effect on Peak Channel Temperature Rise (%)
Vias	100 Hz-10 kHz	+2
Drain & Source Cap Metal	100 Hz-100 kHz	+5
Passivation	100 Hz-8GHz	+32 @ 20MHz
Gate T Metal	1-100 MHz	+25 @ 50MHz
Epi Layers	100 Hz-20GHz	-49 @ 1 MHz

confirmed by steady state simulations. However the effect is significant between approximately 20 kHz and 5 MHz.

IV.   CONCLUSION

Wafer level thermal reliability test structures have been presented which combine gate metal temperature measurement capability and TFR heating. Average gate metal temperature measurements were reported to be in close agreement with 3D FEM simulations. The inclusion of epi layers in the thermal model has been shown to be critical for accurate simulations and their tuning presents a way to apply the thermal model across a range of devices from different fabrication processes. Since the model accounts for the temperature dependent thermal conductivity of the GaAs substrate, the deviations seen in the measurements are attributed to the device bias conditions. In order to improve the accuracy of the thermal simulations a bias dependent correction factor may be used to account for increased heat source localization at higher drain voltages.

An FEM analysis on a full device template using SYMMIC[TM] was compared to a harmonic balance simulation of IMD using a nonlinear device model extracted from electrical measurements. The SYMMIC[TM] simulation and the envelope of the IMD simulation for a device biased in the region near pinch-off were seen to follow the same trend. The low pass transfer function $H(\omega)$ fits well to the SYMMIC[TM] simulation over the frequency range of which the thermal response has a significant effect.
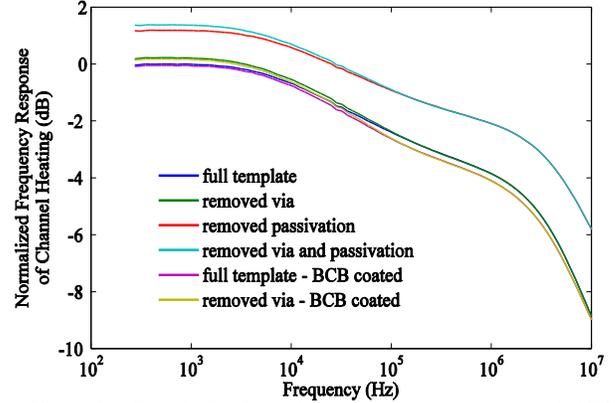
The effects of a device's physical features on its thermal transfer function were also investigated. The greatest amount of device heating was observed when the epi layers were included in the model, while passivation layers provided the most significant level of heat spreading followed by the source and drain cap metal.

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