

## Application Note

# Overcoming Challenges in Integration and Parameterization of EM Simulation Within a High-Frequency Circuit Design Flow

## Overview

Today's complex wireless circuits and systems require the integration of EM simulators into the overall microwave circuit simulation environment in order to successfully design products that meet demand for smaller devices with higher performance in short time-to-market windows. The ability to incorporate multiple EM simulators into one circuit design environment has the obvious advantage of decreased setup time and reduced chance of setup error, which reduces design cycles. There are, however, several challenges for such an integration to be successful. This application note examines some of those challenges and how they can be overcome using NI AWR Design Environment.

Where there is a challenge, there also is an opportunity. NI AWR Design Environment, specifically Microwave Office circuit design software, enables users to quickly take advantage of features such as:

- Multiple process design kits (PDKs) and libraries for different physical technologies
- The ability to drive multiple simulators from one set of layout rules, layer stackup definitions, and shape simplification rules
- The use of 3D cells in 2D layout to support both 3D and 2D layout in one environment
- Easy control of EM simulation results from different simulators using data sets

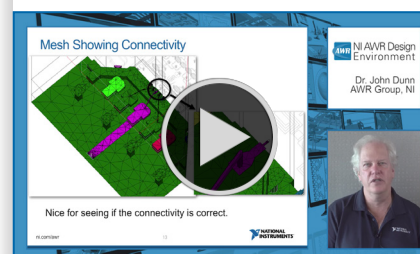
## Setting up an EM Simulation

Designers today have a choice of several different types of EM simulators. They vary by the types of problems they solve and by the way they solve them. Popular EM simulators for microwave engineers are either planar or 3D, depending on the types of geometries they can solve. 3D simulators such as Analyst™, ANSYS HFSS, and CST typically mesh the entire volume of the geometry using some variant of the finite element method (FEM).

Planar simulators solve for currents on metal etched on layers of a dielectric stackup. Vertical vias can also be simulated. While more restrictive in the geometries than the 3D simulators, planar simulators can be used for the most popular manufacturing technologies: chips, boards, and modules. They are widely used because they are usually faster than a 3D simulator to run for applicable geometries. Popular commercial planar simulators include AXIEM and Sonnet.

Several problems immediately present themselves if these simulators are to be supported in one circuit design environment. First, how are planar layout and 3D layout tools supported in the same environment? Second, different simulators have different settings, which would seem to be in direct conflict with the concept of controlling all the simulators from one layout. For example, ports are treated very differently by different simulators. Third, how does the designer work with multiple technologies such as different board, module, and chip stackups?

Watch the related video on AWR.TV  
[youtu.be/XX1nr8QpnFI](https://youtu.be/XX1nr8QpnFI)



## EM Socket II

The new EM Socket™ II architecture within NI AWR Design Environment streamlines design flows between NI AWR software products and third-party EM tools. EM Socket II, the second generation of this technology that was first pioneered by AWR Corporation in the early 2000s, is designed to accomplish four main goals:

- Provide a unified method for setting up EM stackup and material properties for a given process regardless of the EM simulator being used. The designer uses one STACKUP block, which contains all necessary information for the EM simulator.
- Create a single drawing environment for any supported simulator. 3D shapes are included using 3D cells in a 2D layout environment whenever possible. The layout environment supports the use of parameterized cell (PCell) layout, thereby enabling swept parameter and optimized models.
- Support multiple libraries/PDKs for different manufacturing technologies. Board, module, and chip technologies can all be used in the same EM project. This is accomplished by using the concept of hierarchy in the layout. Note that most libraries include layout cells for the various components in the library, for example bond pads, and field-effect transistor (FET) layout cells. EM Socket supports use of these cells.
- It is possible to send layout directly to an EM simulator in EM Socket from the schematic layout using a concept called EM extraction. The designer does not need to redraw the layout; ports are automatically added and the results automatically brought back into the circuit simulator where they replace any models representing the layout.

## Simulation of Multiple Process Technologies

A common problem in 3D EM simulators is the performance of the transition between two different process technologies. For example, the designer might be interested in the transition between a board and a ball grid arrayed module, or between a quad-flat no-leads (QFN) package and a chip by using bond wires. Figure 1a shows a launch from a board, to a QFN package, and then onto a chip using bond wires. The signal leaves Port 1 at the edge of the simulation boundary, travels on the trace on the board, onto the QFN pad, up the bond wire, and ends at Port 2 on the chip. The designer is interested in optimizing the performance of the signal path.

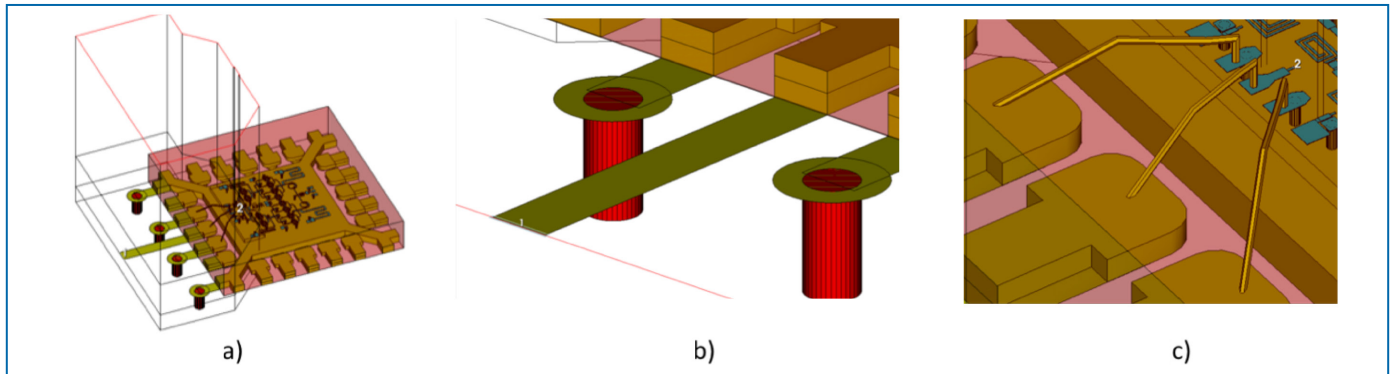


Figure 1: a) MMIC in a QFN package on a Duroid board. The launch has been drawn at Port 1, which goes onto the flat package and then to the MMIC via bond wires at Port 2. b) Grounding vias from the board PDK. c) A close-up of the bond wires.

## Hierarchy

This example uses three different technologies, each with their own materials, layer stackup, and layout cells. At the circuit simulation and layout level, each schematic can work with one PDK describing one technology. For example, the top schematic is used for the board. The various models, design rules, and layout settings are all for the board. Layout cells come from the board PDK. Another schematic is used for the chip design, using a PDK with the corresponding necessary models and layout cells. The schematic describing the chip can be used as a sub-circuit in the design. In this way, the designer can simulate both the board and chip in one simulation.

The S-parameters from the EM simulation of the layout in Figure 1 are needed to describe the transition between the board and the chip. The multiple technologies are again handled in the EM layout using the concept of hierarchy. Different PDKs are used for different cells. Each cell therefore has its own drawing layers and layout cells that can be used. Figure 1b shows an example of two of the grounding vias at the board level.

These vias were drawn by the designer using pre-configured layout cells in the PDK and the signal line was drawn using a PCell in the PDK. The layout, in this case the line, is controlled by parameters. Here, the PCell for the line has parameters for width and length, which can be continuously varied, tuned, and optimized. The ability to include the PDK's PCells in EM layout greatly increases the power of EM Socket.

Eventually, the layout is "flattened" before being sent to the EM simulator, meaning the hierarchy of the layout is removed and the layout consists of the various dielectric layers and shapes of all the sub-cells merged into one layout. The design can therefore send multi-technology layouts through EM Socket to other simulators such as HFSS or CST without worrying about hierarchy and how layout cells are handled. The external simulators are never involved in these issues; it is all handled by EM Socket.

It should be noted that multi-technology type problems work with 3D simulators. Planar simulators require that planar, metal shapes be placed on the dielectric layers of the chip or board. These layers must be infinite in horizontal extent in the case of AXIEM, or go up to the simulation boundary in the case of Sonnet. It is possible to still use hierarchy as an organizational tool for the circuit, but the same technology must be used for all cells.

## Simulating Ports and Boundaries

All EM simulators need ports and the specifics of how the port functions depends on the simulator being used. For example, Analyst 3D simulator can have wave ports at the boundary of the layout and lumped ports inside the simulation space. AXIEM planar simulator, on the other hand, uses an edge port placed at the edge of a piece of metal and has no concept of a wave port, which only exists in 3D simulators. The designer places a port in the EM layout, and its specific properties then depend on the simulator being used. In Figure 1, for example, Port 1 is a wave port when simulated in Analyst. Port 2 on the MMIC could be a lumped port or a wave port, depending on how the designer wants to set up the problem. External simulators support different types of ports. For example, the link to ANSYS HFSS does not support the wave port shown in Figure 1, although it can be manually changed to a wave port later in HFSS.

3D simulators need boundaries at the edges of the simulation region as it is not possible to mesh an infinitely large space. The boundary in EM Socket is drawn as an arbitrary 2D polygon. In Figure 1 the designer drew the boundary to only enclose the region of interest around the board-to-chip transition.

The designer has the ability to choose the specific type of boundary condition to be used on each side of boundary. For this example, perfect conducting walls might be used. An approximate open boundary condition is used for the walls, which attempts to simulate an infinite open region with no walls. It is a numerical analogy to the walls of an anechoic chamber, which is designed to make the walls look invisible to electromagnetic radiation. The specific way in which the approximate open boundary condition is implemented depends on the simulator. Analyst uses the popular 377 ohms/square impedance boundary condition to approximate a perfectly absorbing boundary. It also has options for a more sophisticated perfectly matched layer (PML) boundary condition, in which several thin layers of material are added to the boundary. HFSS and CST have their own variants of these boundary conditions. The results for the board-package-chip launch are shown in Figure 2.

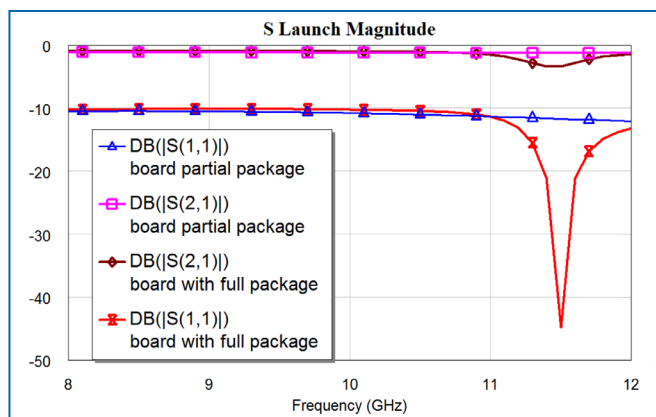


Figure 2: There is a resonance at 11.5 GHz that cannot be seen unless the whole package is simulated.

The magnitude of  $S_{11}$  and  $S_{21}$  in dB are shown for two cases. The traces labeled "board partial package" are the geometry shown in Figure 1. The boundary only encloses the portion of the board, package, and chip relating to the launch study. The second case labeled "board with full package" has a simulation boundary that completely encloses the chip and package. There is an obvious resonance at about 11.5 GHz, which is due to the package becoming half a wavelength long and only being grounded on its periphery. This is a common problem in QFN packaging and designers are usually careful to add some type of grounding vias under the package. The point here is that the designer must remember that when using a boundary enclosing only part of the geometry, any effects of the omitted layout will be neglected.

## 3D and PDK (Library) Cells

The EM socket layout interface is a 2D layout environment, where polygons are placed on drawing layers. The interface needs to support 3D EM tools and therefore 3D objects in layout. There are two ways to make 3D shapes: by extrusion of the polygons or by using 3D cells. Extrusion is a straightforward method in which a 2D polygon is drawn and a vertical distance is specified, either upward or downward.

3D cells are used for the bond wires and the QFN package used in the layout is shown in Figure 1, a close-up of which is shown in Figure 1c. A library of pre-configured 3D cells is included in Microwave Office. The designer simply drags the cell into the layout and places it at the desired location. Vertical positioning and 3D rotation are supported. The layout of most cells is controlled by parameters, for example the number of pads in the QFN package or the length and angle of the bond wires. The philosophy behind 3D cells is that designers of RF and microwave circuits typically only use a small number of 3D cells such as bond wires, BGAs, SMA connectors, and coaxial cables. Typically, their layouts are mainly planar, with the 3D layout regions being between the planar technologies. As an example, a chip-to-package transition with bond wires or BGA technology requires a 3D simulator. The advantage of 3D cells is that the average designer does not need to spend time working in a full-blown 3D layout environment.

EM Socket supports a full 3D editor if needed, enabling the designer to switch over to the 3D layout environment whenever necessary. Suppose a required 3D cell is not available and needs to be created. The designer can create the cell in the 3D editor using parameters where convenient and the cell can be easily inserted into the library of 3D cells for use at a later date. As mentioned earlier, preconfigured layout cells can be included in PDKs, if they are being used. It is even possible for a PDK to include full 3D cells such as a special package or transition used in the given technology. Again, Figure 3 shows the two grounding vias included in the board's PDK.

## Shape Pre-Processing and Simplification

Another feature that is common in the preconfigured libraries supplied within NI AWR Design Environment, specifically Microwave Office software, is shape pre-processing and simplification. When designers run EM and start getting into the layout, typically if they use a manufacturing or mechanical layout there are many features that don't affect the EM. Obviously vias are circular on boards, but, depending on the frequency range and accuracy needed, a square via will do just as well and saves a tremendous number of meshes and therefore simulation time. If the shape pre-processing rules are set up correctly, they can simplify the vias. Figure 3 shows how the vias in EM have become rectangles/squares. It is hard to discern in the image, but in the MMIC they are actually octagons.

Each PDK or technology can have its own preprocessor. Many designers like to use something called "picket fences" on a board, where ground vias are stitched closely together to get better isolation. That is a large amount of meshes, but with shape preprocessing designers can turn the picket fence into one long via wall, which saves a tremendous amount of meshes and yet at the same time gives the same performance in the EM. One of the convenient features about the PDKs in these shape pre-processing rules is that no matter what simulator they are being sent to, the designer can use the same shape simplification.

Figure 4 shows the connectivity feature in EM Socket that is supported by Analyst. There is nothing more frustrating to a user than drawing up a 3D geometry, running it a long time in the simulation, and then discovering that it was not connected correctly. The connectivity feature shows the 3D connectivity, enabling the designer to see that the signal line has not been shorted out.

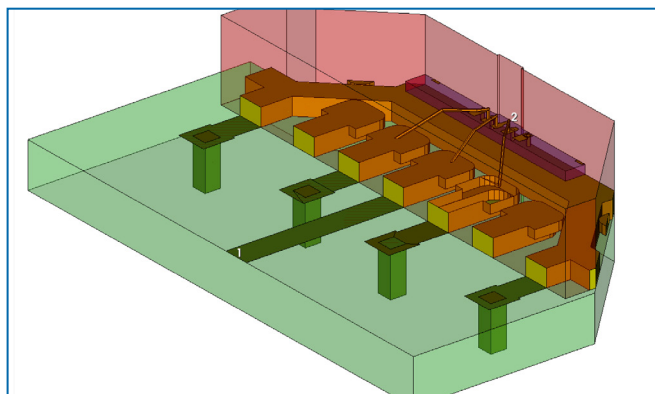


Figure 3: The board vias are square after simplification rules.

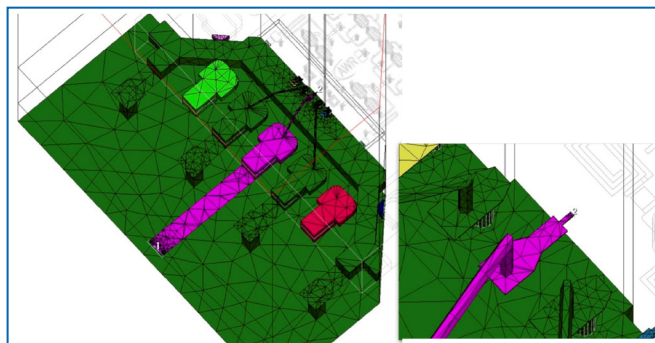


Figure 4: EM Socket connectivity feature, enabling the designer to see if the connectivity is correct.

## EM Extraction

EM extraction enables the designer to send schematic layout directly to an EM simulator, run the simulation, and bring the resulting S-parameters back into the schematic. The circuit simulation with the S-parameters replacing the previous circuit models is rerun and the results in the graphs are updated automatically. The advantage of extraction is the ease of not having to redraw layout, thereby reducing the chance of error in setting up the EM. NI AWR software's extraction flow supports 3D simulators such as Analyst, HFSS, as well as CST.

Turning now to another example, Figure 5 is a MMIC multi-technology module extracted to Analyst. Figure 5a shows the MMIC on a board with connecting bond wires. In the schematic in 5b the elements (thick, finite dielectric blocks, bond wires, boundary, and ports) are selected in red and in 5c the elements are extracted to EM. So the concept of extraction has been extended to 3D simulators, making the extraction process easier, less error prone, and more unified for designers.

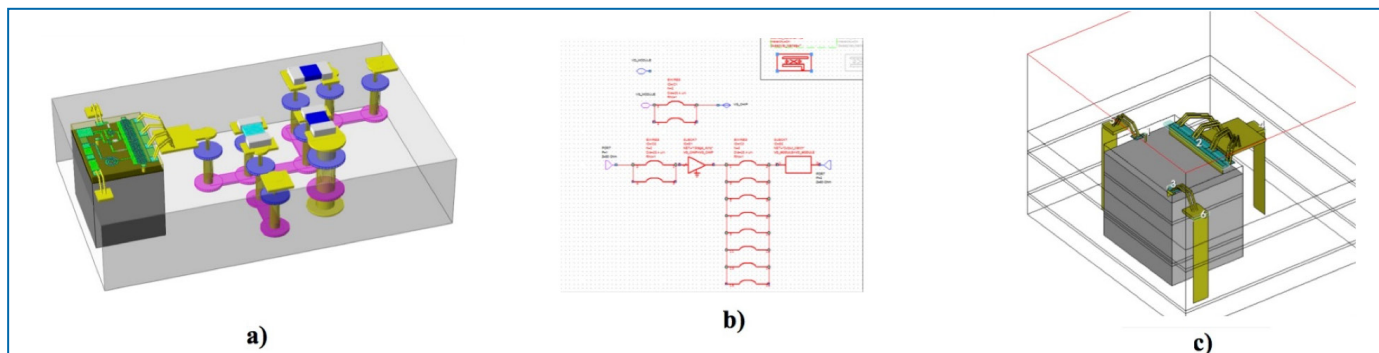


Figure 5: a) MMIC – module multi-technology, b) bond wires selected in the schematic, and c) the extracted transition in Analyst.

## Data Sets of EM Results

Once designers have the results (S-parameter file) from whatever simulator was chosen, they want to be able to easily use those results. NI AWR Design Environment provides data sets to control the versioning of the results so designers can go back and forth quickly between that data. The environment also supports a very tight coupling between the schematic layout and the EM layout, enabling users to create the EM layout from the schematic layout using extraction.

Data sets are now being used for all EM. They store all the old simulation data, enabling designers to quickly swap between data sets, easily control graphs, access prior results to compare current and prior results on graphs, and swap data used by a schematic.

## Conclusion

Today's complex multi-technology designs require multiple simulators, both planar and 3D, and multiple processes. The ability to do circuit and EM simulation in one environment with one setup saves setup time and ensures that all the simulators are getting the same information and the same layout, enhancing accuracy. Controlling multiple EM simulators from within a single environment makes design more powerful and faster because the same PDKs and libraries of PCells and design rules can be used in all simulators and multiple PDKs can be used for different technologies. Finally, the S-parameter results from EM simulations are easy to leverage because they are automatically used in the circuit simulator and the data sets that control the versioning are easy to swap between different results.

NI AWR Design Environment, inclusive of Microwave Office, AXIEM, and Analyst, provides numerous benefits to the designer, including a common user interface, re-use of geometry data, direct embedding of EM results into the circuit hierarchy, and powerful pre-processing capabilities that can be carried out before the EM project is simulated.

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